Source/Drain Asymmetry in InGaAs Vertical Nanowire MOSFETs

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***Abstract*— This paper demonstrates InGaAs vertical nanowire (VNW) MOSFETs fabricated via an improved top–down approach, the performance of which is comparable to that of the best bottom–up devices in terms of the balance between transport and electrostatics. These devices, when contrasted with an earlier generation fabricated by a similar technology, have enabled the first experimental study of source/drain asymmetry in InGaAs VNW MOSFETs. The transconductance differs significantly when swapping source and drain due to inherently different top and bottom contact electrical resistance. This also results in distinct asymmetry in the saturation behavior of the output characteristics. On the other hand, diameter nonuniformity along the nanowire (NW) length is responsible for asymmetry in the subthreshold characteristics. A uniform NW cross section, enabled by our improved InGaAs dry etch technology in the present devices, eliminates the asymmetry of the electrostatics, which was observed in our previous work.**

***Index Terms*— Digital etch, InGaAs, MOSFETs, nanowire (NW), reactive ion etching, top–down, vertical channel.**

I. Introduction

InGaAs is considered a promising material candidate for CMOS technologies beyond the 10-nm node [1], [2]. These deeply scaled technologies will require not only new channel materials but also a highly 3-D transistor structure. A nanowire (NW) channel with a wrap-around gate is regarded as the ultimate CMOS device architecture [3]. Recent circuit-level modeling has shown that vertical NW (VNW) MOSFETs offer better performance, occupy smaller area, and consume less power than conventional horizontal NW MOSFETs [4]. This advantage is attributed to the relaxed gate length, spacer thickness and contact length scaling that the vertical geometry affords as opposed to the very tight contacted-gate pitch constraints of horizontal devices. Combining a high-mobility channel material such as InGaAs with a VNW transistor geometry is particularly interesting as the relaxed gate length scaling that it enables can alleviate direct source-to-drain tunneling prominent in InGaAs MOSFETs in these ultrascaled dimensions [5]. In addition, the VNW geometry opens the door for heterojunction engineering in the transport direction, which can potentially reduce the gate-induced drain leakage [6].

InGaAs VNW MOSFETs have been demonstrated by bottom–up [7] and top–down approaches [8], [9]. Recently, remarkable improvement in device performance has been achieved using a bottom–up technique [10]. In this paper, we present transistors fabricated by an improved top–down approach, the results obtained for which match the recent results. This has been obtained through a fabrication process that features an enhanced InGaAs dry etch technology with superior profile control [9], a scaled gate oxide, and an improved oxide/semiconductor interface.

Our latest VNW transistor technology reported here, when compared with an earlier transistor generation [8], has allowed us to study the impact of asymmetry of VNW InGaAs MOSFETs, an issue of great importance to circuit designers. This is a topic that has been investigated theoretically [11] but has not been studied experimentally in the InGaAs system. This represents an important gap because VNW transistors are intrinsically asymmetric to source–drain (S/D) swapping, in contrast with intrinsically symmetric horizontal devices.

We find that asymmetry in transistor electrical characteristics arises from the difference between the top and bottom contacts as well as the shape of the sidewall profile. The difference in contact resistance impacts the ON-current characteristics. A nonuniform NW diameter affects the saturated subthreshold characteristics, in particular drain-induced barrier loweirng (DIBL). This is in agreement with theoretical studies [11]. Compared to our previous work [8], our latest etching technology delivers highly vertical sidewalls along the entire active region which largely eliminates the asymmetry in electrostatics.

II. Experiment

Fig. 1 shows the schematic cross section of our latest generation of VNW MOSFETs. The starting heterostructure, consists of an 80-nm undoped $In_{0.53}Ga_{0.47}As$ channel sandwiched between two n^+ contact regions. The major difference between the heterostructure used in this paper and that of our previous work [8] is the design of the contact region, now featuring a highly doped composite gap that consists of (from top) 7-nm $In_{0.53}Ga_{0.47}As$/ 2-nm InAs/ 6-nm $In_{0.7}Ga_{0.3}As$ on top of 55-nm $In_{0.53}Ga_{0.47}As$ (all layers are n^+-doped with Si). This is in contrast with 70-nm n^+ $In_{0.53}Ga_{0.47}As$ used in [8].

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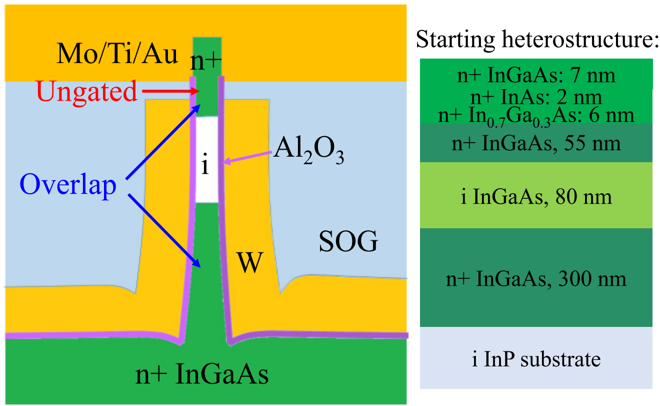

Fig. 1. Schematic of device structure and starting heterostructure.

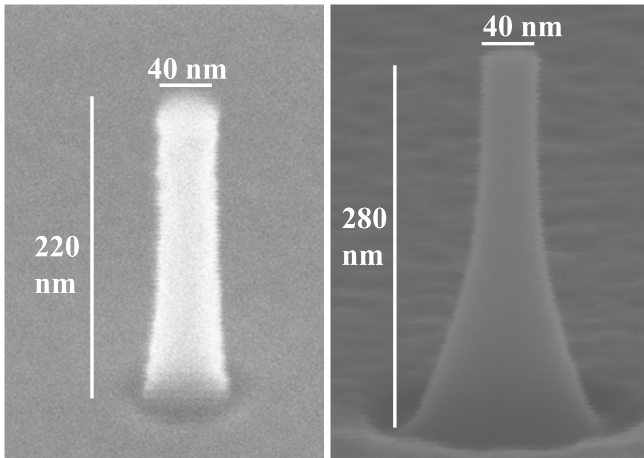

Fig. 2. Improved NW profile in this paper (left) compared to previous work [8] (right).

The new design was intended to reduce the contact resistance as InGaAs is reported to form better ohmic contacts when the InAs composition is high [12].

Device fabrication follows our previous work [8] but it incorporates a number of innovations. NW etching is realized through an improved InGaAs dry-etch technology [9] that yields nearly vertical and smooth sidewalls and a very uniform NW diameter (Fig. 2, left). This was obtained by increasing the substrate temperature during etch and optimizing the etching conditions (gas flow ratio, etc.,) In addition, our latest process features a scaled gate oxide consisting of 3 nm of Al_2O_3 [$\sim$1.5-nm equivalent oxide thickness (EOT)] and greater attention to atomic layer deposition conditioning to improve the quality of the oxide semiconductor interface. Ten cycles of digital etch [13] were employed to trim the NW diameter (D) and improve the quality of the semiconductor/oxide interface [9]. The final device features a single NW with a channel length (L_{ch}) of 80 nm (the intrinsic InGaAs layer thickness) and diameter $D = 40$ nm.

III. Results and Discussion

The output, subthreshold, and transconductance characteristics (measured with bottom electrode as the source) of an exemplary device are shown in Figs. 3 and 4 in black. The linear ($V_{ds} = 0.05$ V) and saturated ($V_{ds} = 0.5$ V) subthreshold swings (S_{linear} and S_{sat}) are 98 and 114 mV/decade, respectively, while DIBL is 177 mV/V. A peak transconductance ($g_{m,pk}$) of 620 μS/μm is achieved with an ON resistance of 895 $\Omega\cdot\mu$m (both normalized to the NW diameter). The drain current fluctuations in Figs. 3 and 4 are attributed to discrete charge trapping events via the very few oxide and interface defects [14] in single NW devices due to their extremely small channel area.

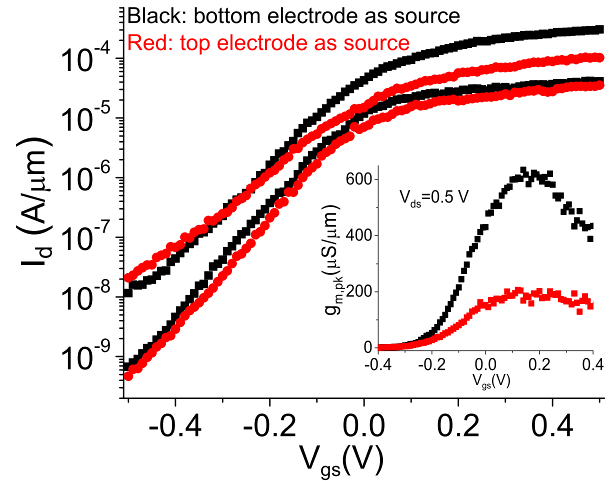

Fig. 3. Subthreshold characteristics of an exemplary device measured with bottom electrode at the source (BES, black) versus top electrode as the source (TES, red). Inset: transconductance characteristics.

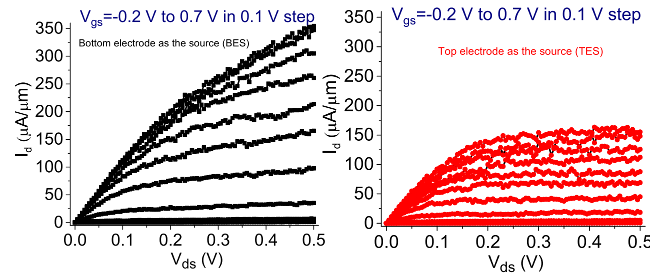

Fig. 4. Output characteristics measured with BES versus TES of the device shown in Fig. 3.

Fig. 5 benchmarks the transport and electrostatics in recently published InGaAs VNW MOSFETs by plotting $g_{m,pk}$ versus minimum S_{sat}, both at $V_{ds} = 0.5$ V. This graph highlights the tradeoff that often exists between transport and electrostatics. The results presented in this paper (orange star) demonstrate a significant improvement in the electrostatics of top–down fabricated devices when compared to our previous results (green triangles) [8]. This is mainly due to the scaled gate oxide and the improved oxide/semiconductor interface. Our newest results match the best results recently obtained following a bottom–up fabrication approach [10].

Our fabrication process yields many working devices with relatively well behaved electrical characteristics. This has allowed us to carry out a study of device asymmetry and its impact on electrical figures of merits (FOM). We have performed device electrical measurements by swapping source and drain. The characterization procedure is benign

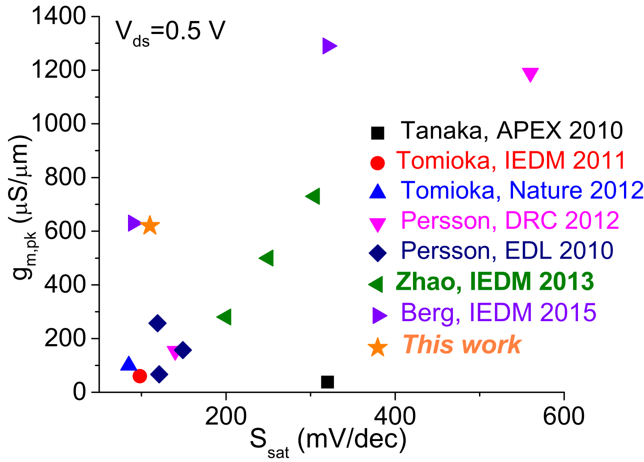

Fig. 5. $g_{m,\mathrm{pk}}$ versus minimum saturated S at $V_{\mathrm{ds}} = 0.5$ V for vertical InGaAs and InAs NW MOSFETs. A tradeoff is evident in terms of electrostatics and transport.

and the device characteristics remain stable after repeated measurements.

A typical example of the impact of S/D swap is shown in Figs. 3 and 4, where measurements with bottom electrode as the source (BES, black) and top electrode as the source (TES, red) are plotted. We see that the subthreshold behavior barely changes while the ON current at $V_{\mathrm{ds}} = 0.5$ V is greatly affected. The asymmetry in the ON regime can be quantified by the change in peak transconductance which is 620 μS/μm for BES versus 200 μS/μm for TES (inset of Fig. 3).

This strong asymmetry in ON characteristics can be attributed to the significant difference in series resistance at the bottom and at the top of the NW. In our NW devices, the contact to the top electrode only covers the pillar tip, a very small area. The contact to the bottom electrode, on the other hand, takes place on the bottom conductive plane and has a much larger contact area. As a result, the top contact presents much more resistance than the bottom contact. In consequence, the TES configuration offers a small drain resistance R_d and a large source resistance R_s, while BES gives a small R_s and large R_d. It is well established that R_s has a much larger effect on extrinsic g_m than R_d [15], and this results in significantly higher g_m for BES with respect to TES.

In fact, the top contact is a major roadblock to VNW MOSFETs due to the small area available. Even with a doping level as high as 3×10^{19} cm^{-3}, the depletion width underneath the Mo contact in InGaAs approaches 5 nm. The implication is that NWs with sub-10 nm diameter could be fully depleted under the contacts. To alleviate this problem, process and device engineering efforts at the top semiconductor/metal contact are required, using methods such as a longer contact length, wider NW diameter at the top or Schottky barrier height engineering. In the future scaled technologies with a tight pitch, the bottom contact may also add significant series resistance due to the constraint on the via size and the lateral access resistance [4]. Addressing this will require novel process and device design.

Fig. 4 compares the output characteristics of the device in Fig. 3 in both configurations. As expected, R_{ON} is roughly the same in both configurations (895/897 $\Omega\cdot\mu$m for BES/TES). However, in addition to the difference in maximum current already discussed, TES enables better saturation than BES. This is a consequence of the smaller R_d under TES.

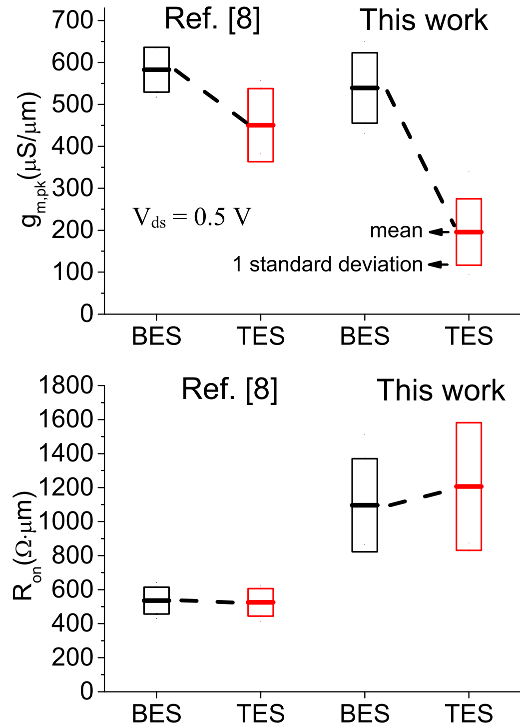

Fig. 6. $g_{m,\mathrm{pk}}$ and R_{ON} asymmetry for devices from our previous work [8] and this paper.

In an FET, the intrinsic drain-to-gate voltage $V_{\mathrm{dg},i}$ establishes the saturation of the device output characteristics. For example, in a classic long channel MOSFET, drain current saturation happens around $V_{\mathrm{dg},i} = -V_t$. In the presence of series drain and source resistance, $V_{\mathrm{dg},i}$ differs from the extrinsic drain-to-gate voltage V_{dg} and is given by

$$\boldsymbol{V}_{\mathrm{dg},i} = \boldsymbol{V}_{\mathrm{dg}} - \boldsymbol{I}_d \times \boldsymbol{R}_d. \tag{1}$$

This means that, to the first order, the drain resistance contributes to the reduction of $V_{\mathrm{dg},i}$ but the source resistance does not. In consequence, high R_d hampers device saturation while high R_s does not. In our devices in the TES configuration, $R_s \gg R_d$ while in the BES configuration, $R_d \gg R_s$. As a result, the TES configuration exhibits better current saturation than the BES configuration.

Fig. 6 compares the behavior of ON regime FOM, transconductance and R_{on}, in the BES and TES configurations for the present run and the devices in [8]. As is reasonable to expect, there is no asymmetry in R_{on}. We can see, however, that there is strong asymmetry in $g_{m,\mathrm{pk}}$ in this paper. Also, $g_{m,\mathrm{pk}}$ here is comparable to our previous result [8] in the BES configuration, despite a scaled EOT (1.5 versus 2.2 nm). This is mainly due to the increased resistance of the top contact in the present devices. The cause of this is hypothesized to be a lower doping of the n$^+$ contact layers caused by reduced cracking of the Si_2H_6 precursor at the reduced epitaxial growth temperature of 450 °C. The increased top contact resistance

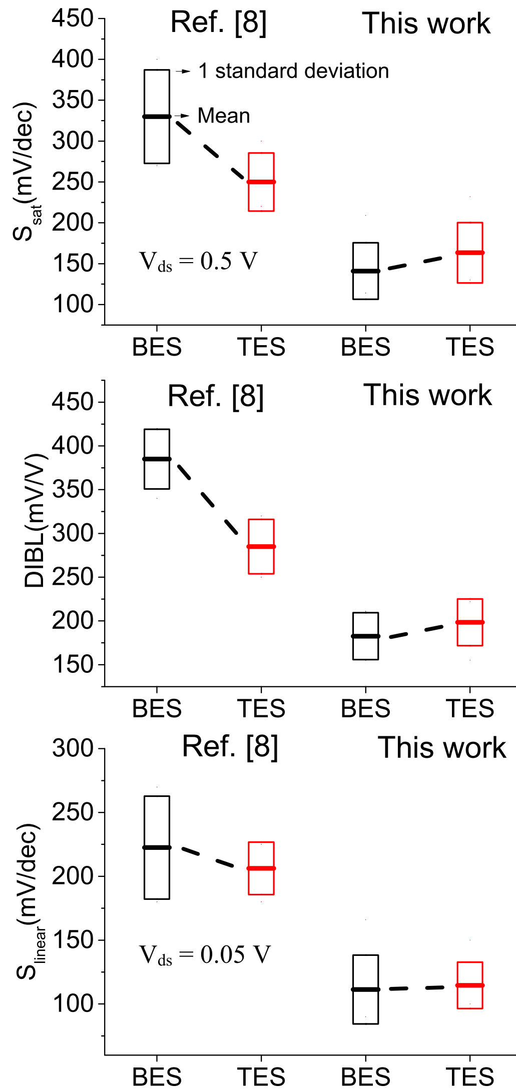

Fig. 7. Asymmetry of the subthreshold characteristics for devices from our previous work [8] and this paper.

also contributes to the greater g_m asymmetry observed in this paper and the sharp increase in R_{on}.

In addition to asymmetry in the ON regime, there is also asymmetry in the subthreshold characteristics to consider. This was very prominent in our previous devices [8] but has been eliminated in the present ones. This is shown in Fig. 7. This graph plots key FOM values pertaining to subthreshold characteristics for devices from our previous work [8] and our current work. For DIBL and S_{sat}, our previous devices displayed significant asymmetry. As discussed theoretically in [11], DIBL and S_{sat} are primarily determined by the NW diameter at the source which is about 15 nm wider in the BES configuration with respect to the TES configuration in the devices in [8]. In the present paper, our improved dry etch technique leads to a much more uniform NW cross section (Fig. 2). This results in the suppression of DIBL and S_{sat} asymmetry. Also, consistent with simulations in [11], S_{linear} does not reveal significant asymmetry in either chip.

IV. Conclusion

We have demonstrated top–down InGaAs VNW MOSFETs with comparable performance to the best bottom–up devices in terms of the balance between electrostatics and transport. In addition, S/D asymmetry inherent to VNW MOSFETs has been experimentally studied for the first time. Improved NW sidewall profile enabled by our optimized dry etch technology suppresses the asymmetry in electrostatics. We show that asymmetry in g_m and output characteristics arise from the inherent asymmetry in the top and bottom contacts.

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